Non-Responsive Document
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Exhibit D

EXHIBIT D

OFGS File No.: IR 2.064 (2-838)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:	
ALEXANDER LIDOW et al.	
Patent No.: 5,008,725	
Reexamination Control No.: 90/003,495	NON-RESPONSIVE AMENDMENT PURSUANT TO 37 C.F.R. § 1.550(b)
Filing Date: July 15, 1994	
Examiner: CARROLL, J.	
Group Art Unit: 2508	

Box Reexam
Hon. Commissioner of
Patents and Trademarks
Washington, DC 20231

Transmitted herewith is an amendment in the above-identified reexamination.

OFGS Check No. 4003, which includes the fee of $ 568.00, calculated below, is attached.

NO. CLAIMS AFTER AMENDMENT		HIGHEST NO. PREVIOUSLY PAID FOR		EXTRA PRESENT		RATE	ADDIT. FEE
TOTAL 35	MINUS	23*	=	12	x	($11 SE or $22)	$ 264
INDEP. 8	MINUS	4**	=	4	x	($38 SE or $76)	$ 304
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM***					x	($120 SE or $240)	$
						TOTAL	$ 568

* patent issued with total of 23 claims (including multiple dependencies)
** patent issued with 4 independent claims
*** multiple dependent claims were previously presented in patent

In the event the actual fee is greater than the payment submitted or is inadvertently not enclosed or if any additional fee during the prosecution of this application is not paid, the Patent Office is authorized to charge the underpayment to Deposit Account No. 15-0700.

If this communication is filed after the shortened statutory time period had elapsed and no separate Petition is enclosed, the Commissioner of Patents and Trademarks is petitioned, under 37 C.F.R. §1.136(a), to extend the time for filing a response to the outstanding Office Action by the number of months which will avoid abandonment under 37 C.F.R. §1.135. The fee under 37 C.F.R. § 1.17 should be charged to our Deposit Account No. 15-0700.

Respectfully submitted,

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In re Patent of:

ALEXANDER LIDOW et al.

Patent No.: 5,008,725

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NON-RESPONSIVE
AMENDMENT PURSUANT TO
37 C.F.R. § 1.550(b)

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Hon. Commissioner of
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Washington, DC 20231

Sir:

Please amend claims 1, 3, 7 and 8 of U.S. Patent No. 5,008,725 back to their original unamended form as follows:

1. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of symmetrically disposed laterally distributed identical hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface;

said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;

a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

a drain electrode connected to said second planar surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

3. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of symmetrically disposed laterally distributed identical polygonal base regions each having a second conductivity type formed in said lightly doped region and extending for a given depth beneath said first planar semiconductor surface;

said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to

form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

a drain electrode connected to said second planar semiconductor surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

7. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted; the space between adjacent ones of said polygonal base regions defining a common conduction region of

said first conductivity type extending downwardly from said first planar semiconductor surface;

a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface; and

a drain electrode coupled to said drain conductive region.

8. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar

semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

the surface of said common conduction region being continuous and uninterrupted and of said first conductivity type;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semi-conductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separate therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

each of said at least first and second spaced base regions having identical polygonal configurations; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region.

Please delete proposed claims 15-18 as filed in the Amendment filed on March 24, 1995 and replace those claims with the following new proposed claims 15-18:

15. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of equally spaced symmetrically disposed laterally distributed identical hexagonal base regions each having a second conductivity type formed in said epitaxially deposited region and extending for a given depth beneath said first planar surface, the space between said hexagonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar surface;

said hexagonal base regions spaced at said first surface from surrounding ones by a symmetric hexagonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said hexagonal base regions being parallel to an adjacent side of another of said hexagonal base regions;

a hexagonal annular source region of said first conductivity type formed in an outer peripheral region of each of said hexagonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective hexagonal base region to

form an annular channel between each of said outer rims of said annular source regions and said symmetric hexagonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective hexagonal base regions;

a drain electrode connected to said second planar surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

16. The device of claim 15 wherein said vertical common conduction region is disposed beneath said insulation layer means on said first surface.

17. A high power MOSFET device having more than 1000 parallel-connected individual FET devices closely packed into a relatively small area comprising:

a thin wafer of semiconductor material having first and second spaced, parallel planar surfaces; at least a first portion of the thickness of said wafer which extends from said first planar surface consisting of an epitaxially deposited region of a first conductivity type;

a plurality of equally spaced symmetrically disposed laterally distributed identical polygonal base regions each having a second conductivity type formed in said lightly doped region and extending for a given depth beneath said first planar semiconductor surface, the space between said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar surface;

said polygonal base regions spaced at said first surface from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted;

each side of each of said polygonal base regions being parallel to an adjacent side of another of said polygonal base regions;

a polygonal annular source region of said first conductivity type formed in an outer peripheral region of each of said polygonal base regions and extending downwardly from said first planar surface to a depth less than the depth of said base regions;

an outer rim of each of said annular source regions being radially inwardly spaced from an outer periphery of its respective polygonal base region to form an annular channel between each of said outer rims of said annular source regions and said symmetric polygonal lattice of semiconductor material of said first portion of said wafer;

a common source electrode formed on said first planar surface and connected to a plurality of said annular source regions and to interiorly adjacent surface areas of their said respective polygonal base regions;

a drain electrode connected to said second planar semiconductor surface of said wafer;

an insulation layer means on said first planar surface and overlying at least said annular channels; and

a polysilicon gate electrode atop said insulation layer means and operable to invert said annular channels.

18. The device of claim 17 wherein said vertical common conduction region is disposed beneath said insulation layer means on said first surface.

Please add the following new proposed claims 21-26:

21. A vertical conduction high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising:

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

a plurality of highly packed, equally spaced symmetrically disposed identical polygonal base regions of a second conductivity type formed in said wafer, each extending from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; said polygonal base regions spaced from surrounding ones by a symmetric polygonal lattice of semiconductor material of said first conductivity type;

said lattice being continuous and uninterrupted; the space between adjacent ones of said polygonal base regions defining a vertical common conduction region of said first conductivity type extending downwardly from said first planar semiconductor surface;

a respective polygonal annular source region of said first conductivity type formed within each of said polygonal base regions and extending downwardly from said first planar semiconductor surface to a depth less than said first depth; each of said polygonal annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define respective coplanar annular channel regions along said first planar semiconductor surface between the polygonal sides of each of said polygonal annular source regions and said common conduction region;

a common source electrode means connected to said polygonal annular source regions and their respective base regions;

gate insulation layer means on said first planar semiconductor surface, disposed at least on said coplanar channel regions;

gate electrode means on said gate insulation layer means and overlying said coplanar channel regions;

a drain conductive region remote from said common conduction region and separated therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface; and

a drain electrode coupled to said drain conductive region.

22. The device of claim 21 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

23. The device of claim 21 wherein said drain electrode is connected to said second semiconductor surface.

24. A high power MOSFET device exhibiting relatively low on-resistance and relatively high breakdown voltage; said device comprising;

a wafer of semiconductor material having planar first and second opposing semiconductor surfaces; said wafer of semiconductor material having a relatively lightly doped major body portion for receiving junctions and being doped with impurities of a first conductivity type;

at least first and second spaced base regions of a second conductivity type formed in said wafer and extending downwardly from said first planar semiconductor surface to a first depth beneath said first planar semiconductor surface; the space between said at least first and second spaced base regions defining a vertical common conduction region of a first conductivity type at a given first planar semiconductor surface location; said common conduction region extending downwardly from said first planar semiconductor surface;

the surface of said common conduction region being continuous and uninterrupted and of said first conductivity type;

first and second annular source regions of said first conductivity type formed in said first and second spaced base regions respectively at said first planar semiconductor surface locations to a depth less than said first depth; said first and second annular source regions being laterally spaced along said first planar semiconductor surface from the facing respective edges of said common conduction region thereby to define first and second channel regions along said first planar semiconductor surface between each pair of said first and second annular source regions, respectively, and said common conduction region; each of said first and second channel regions being coplanar with one another;

a common source electrode means connected to said first and second annular source regions and their respective first and second base regions;

gate insulation layer means on said first planar semi-conductor surface, disposed at least on said first and second channel regions;

gate electrode means on said gate insulation layer means and overlying said first and second channel regions;

a drain conductive region remote from said common conduction region and separate therefrom by said relatively lightly doped major body portion and extending to said second semiconductor surface;

a drain electrode coupled to said drain conductive region; and

each of said at least first and second spaced base regions having identical polygonal configurations; each of said first and second annular source regions having a polygonal configuration conforming to that of their respective base region.

25. The device of claim 24 wherein said vertical common conduction region is disposed beneath said gate insulation layer means on said first surface.

26. The device of claim 24 wherein said drain electrode is connected to said second semiconductor surface.

REMARKS

The foregoing Amendment is submitted pursuant to 37 C.F.R. § 1.550(b) to place proposed amended claims 1, 3, 7 and 8 back to their original unamended form (i.e. as set forth in the Reexamination Certificate issued on April 16, 1991). The proposed amendments to claims 1, 3, 7 and 8 submitted in the Amendment filed on March 24, 1995 are now recited instead in new proposed independent claims 15, 17, 21 and 24.

New proposed dependent claims 15-18 as submitted in the Amendment filed on March 24, 1995 have been renumbered as new claims 16, 18, 22, and 25, respectively, in the foregoing Amendment. New proposed claims 19 and 20 remain dependent on claims 7 and 8, respectively (now presented in their original, unamended form), and have also been added as new dependent claims 23 and 26 (dependent on new proposed independent claims 21 and 24, respectively).

The foregoing Amendment and remarks are not responsive to the Office Action mailed on May 17, 1995. A responsive submission will be filed on or before expiration of the two month shortened statutory period for response on July 17, 1995.

Date: May 25, 1995

Respectfully submitted,

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CERTIFICATE OF SERVICE

The undersigned hereby certifies that a true and correct copy of the foregoing "NON-RESPONSIVE AMENDMENT PURSUANT TO 37 C.F.R. § 1.550(b)" is being served on the attorneys for Requester SGS-Thomson Microelectronics, Inc. by sending a true copy of such document by first class mail, postage prepaid, on May 25, 1995 to the address set forth below.

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